Enhancing IBIS to support
frequency and voltage dependent
Final Stage
by adding a new IBIS keyword
Final_Stage_Subckt

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October 21, 2008

Final_Stage_Subckt

The goal is to specify a Spice subckt to be used instead of C_Comp by adding a new [Model] keyword Final_Stage_Subckt.

1. IBIS record
    a. Final_Stage_Subckt <corner> <file name> <subckt name>
        i. <corner>
            1. typ   Typical
            2. min   Slow
            3. max   Fast
        ii. <file name>
            1. Name of file containing Spice subckt
        iii. <subckt name>
            1. Name of Spice subckt
    b. Diff_Final_Stage_Subckt <corner> <file name> <subckt name>
        i. Same as above
2. Rules of Spice subckt contents
    a. Written in IBIS Buffer Spice
        i. IBIS Buffer Spice is a superset of IBIS Interconnect Spice with additions such as table driven resistor and capacitor elements.
    b. Final_Stage_Subckt first non-comment line shall be:
        i. .subckt <subckt> <p1> <p2> <ground> <power> <corevdd> <vref> <stimulus> <enable>
            1. <subckt>
                a. subckt name
            2. <p1>
                a. pad on B element side of model
            3. <p2>
                a. pad on package side of model
            4. <ground>
                a. Buffer ground node
            5. < power >
                a. Buffer power node
            6. <corevdd>
                a. Buffer core power node
            7. <vref>
                a. Buffer switching reference node
            8. <Stimulus>

a. If Output or IO
b. Stimulus node
    i. Non inverting
        1. 0V=low, 1V=high
    ii. Inverting
        1. 1V=low, 0V=high

9. \<Enable\>
    a. If IO or Tristate
    b. Enable node
        i. Active High
            1. 0V=Un-enabled, 1V=Enabled
        ii. Active Low
            1. 1V= Enabled, 0V= Un-enabled

c. Diff_Final_Stage_Subckt first non-comment line shall be:
    i. .subckt \<subckt\> \<p1_H\> \<p1_L\> \<p2_H\> \<p2_L\> \<ground\> \<power\> \<corevdd\> \<vref\> \<stimulus\> \<enable\>
d. Last non-comment line shall be either:
    i. .ends
    ii. .ends \<subckt name\>

3. When Final_Stage_Subckt is used in a simulation, then C_Comp should not be used.

Implementation of "Branches"

.subckt branches pad_ibis pad_package
+ ground power corevdd vref stimulus enable
*
* Make sure that nodes unused in this model are not hanging
R_power power 0 1Meg
R_corevdd corevdd 0 1Meg
R_vref vref 0 1Meg
R_stimulus stimulus 0 1Meg
R_enable enable 0 1Meg
*
* Shunt connection between two "pad" nodes
V_shunt pad_ibis pad_package DC=0
*
* pad_ibis --- R_Comp --- inode --- C_comp --- Ground
*
* R_Comp
R_rcomp pad_ibis inode V(vrcomp)
E_rcomp vrcomp inode PWL(1) vrcomp inode (.1,0v .2,1v .5,4v)
*
* C_Comp
C_comp inode ground V(vccomp)
E_ccomp vccomp ground PWL(1) inode ground (1p,0v 1p,1v 5p,4v)
*
.ends branches

Differential Final Stage

```
.subckt diff_term
+ pad_ibis_H pad_ibis_L pad_package_H pad_package_L
+ ground power corevdd vref stimulus enable
*
* Make sure that nodes unused in this model are not hanging
R_power power 0 1Meg
R_corevdd corevdd 0 1Meg
R_vref vref 0 1Meg
R_stimulus stimulus 0 1Meg
R_enable enable 0 1Meg
*
* Shunt connection between two "pad" nodes
V_shunt_H pad_ibis_H pad_package_H DC=0
V_shunt_L pad_ibis_L pad_package_L DC=0
*
R_term_H  pad_ibis_H vref 50
R_term_L  pad_ibis_L vref 50
*
.ends diff_term
```